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JAN 23 2002  
PATENT & TRADEMARK OFFICE  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No.: M4065.0127/P127-A  
(PATENT)

In the Patent Application of:  
Kye Y. Ahn, et al.

Application No.: 09/660,324

#8/C  
1/29/02  
Group Art Unit: 2823

Confirmation No.: 2581

Filed: September 12, 2000

Examiner: F. Toledo

For: SILICON MULTI-CHIP MODULE  
PACKAGING WITH INTEGRATED  
PASSIVE COMPONENTS AND METHOD  
OF MAKING

RECEIVED  
JAN 25 2002  
TC 2800 MAIL ROOM

AMENDMENT

Box Non-Fee Amendment  
Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In response to the non-final Office Action dated November 26, 2001 (Paper No. 7), please amend the above-identified U.S. Patent application as follows:

IN THE CLAIMS:

88 (amended) A process for forming an interposer element for use as a chip carrier comprising the steps of:  
Circuit  
E  
providing an insulating layer on at least one surface of a silicon substrate; and